520.43079X00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: TANAKA, et al.

Filed: August 27, 2003

For: SYSTEM AND METHOD FOR EVALUATING A SEMICONDUCTOR DEVICE PATTERN, METHOD FOR CONTROLLING PROCESS OF FORMING A SEMICONDUCTOR DEVICE PATTERN AND METHOD FOR MONITORING A SEMICONDUCTOR DEVICE MANUFACTURING PROCESS

CLAIM FOR PRIORITY

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

August 27, 2003

Sir:

Under the provisions of 35 USC §119 AND 37 CFR § 1.55, Applicants hereby claim the right of priority based on Patent Application No. 2003-033522 filed in Japan on February 12, 2003.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP

for William I. Solomon 22973
Registration No. 28,565

1300 North Seventeenth Street
Suite 1800
Arlington, VA 22209
Tel.: 703-312-6600
Fax: 703-312-6666
WIS/alb